REMARKS

Present Status of the Application

Upon entry of the amendments in this response, claims 1-16 are pending of which claims 1,2 and 9 have been amended, as instructed by the examiner, without prejudice or disclaimer in order to more explicitly describe the claimed invention. It is believed that no new matter is added by way of amendments made to the claims. For at least the foregoing reason, applicants respectfully submit that claims 1-16 patently define over prior art of record and reconsideration of this application is respectfully requested.

Discussion for objection to claims 1,2 and 9 under 35 U.S.C. 112 2nd paragraph

1.Claims 1 recites the undefined term, "cos(i,k)" and claim 2 recites the ambiguous term, 'efficient memory."

In response thereto, applicants appreciate the examiner's pointing out these informalities. Therefore, the claims 1 and 2 have been amended as instructed by the examiner so as to eliminate these claims' informalities. Meanwhile, the claim 9 has the same informalities as the claim1 and accordingly is amended.

Discussion for objection to claims under 35 U.S.C.103(a)

1. *Claims 1,6-9, and 14-16 are rejected under 35 U.S.C.103(a) as being unpatentable over Tsai et al.("Implementation Strategy of MPEG-2 Audio Decoder and Efficient Multi-channel Architecture", hereinafter referred to "Tsai1") in view of Sakamoto etal.("A fast MPEG Audio layer III algorithm for 32-bit MCU"), and ISO/IEC-3.*

As per claims 1,8 and 9

ISO/IEC-3 teaches IMDCT, windowing and overlap-add functions for MPEG layer III. Further Sakamoto teaches in order to carry out the MPEG layer-3. a number of multiplications and additions per frame are needed(multiply-add operations are required, p988, col. 1 paragraph 3.1, lines 1-2).

Moreover, Tsai 1 and Sakamoto do not disclose a register stack. However, ISO/IEC-3 specifies that for overlapping and adding with previous block to occur, the second half of the actual block is stored to be used in the next block (p37, heading 2.4.3.4.10.4., lines 1-2)

Finally, Tsai does not teach storing the DWIMDCT result in a buffer memory, However, Tsai teaches an IMDCT buffer (IMDCT buffer, p 297, Fig.5). Therefore, it would be obvious for one of ordinary skill in the art to include the register stack taught by ISO/IEC-3 and the number of multiplier-adder taught by Sakamoto into the MPEG layer-2 decoder of the Tsai 1. As a result, claims 1,8 and 9 are unpatentable under 35 U.S.C.103(a).

In response thereto, applicants respectfully transverse the aforementioned objections based on the following arguments and thus withdrawal of objections to the claims 1, 8 and 9 is respectfully requested.

First of all, applicants would like to point out the author of "Tsai1" , "Tsai 2" and the inventor of the present invention is the same person. To establish a prima facie case of obviousness, the cited references (here referring to Tsai1, Sakamoto and ISO/IEC-3) should disclose all limitations of claims 1, 8 and 9. That is, even Sakamoto discloses a number of multiplications and additions and ISO/IEC-3 specifies that the second half of the actual block is stored to be used in the next block, ISO/IEC-3 fails to disclose where the second half of the

actual block to be stored. It would be inappropriate that the examiner presumed that the second half of the actual block to be stored into the same register stack as the present invention because the examiner's presumption has no ground. Even if the examiner's presumption is valid, the register stack of the present invention does function to store the result of IMDCT, rather than the result of the overlap-add operation as disclosed in ISO/IEC-3. Moreover, the examiner alleged that Tsai1 teaches an IMDCT buffer; however, as described in [00024] in lines 5-7 in the specification, the DWIMDCT buffer memory 32 claimed in the independent claims 1 and 8 is used to store the result of the overlap-add of dynamic window (i.e. DWIMDCT). As a result, DWIMDCT buffer memory of the present invention has a distinct function from that of Tsai1.

Accordingly, neither Tsai 1, Sakamoto and ISO/IEC-3 or combinations thereof teach, suggest or disclose "an operation result of the inverse-modified discrete cosine transform is stored in a register stack..; and an operation result of the overlap-add is stored in a DWIMDCT buffer memory." as claimed and featured in independent claim1. Likewise, neither Tsai 1, Sakamoto and ISO/IEC-3 or combinations thereof teach, suggest or disclose "a register stack, used to store an operation result of the inverse-modified discrete cosine transform; and a DWIMDCT buffer memory, used to store an operation result of the overlap-add." as claimed in the independent claim 8. Furthermore, from section 3.1 in Sakamoto, it employs a great number

of multily-asdd operations in MP3 decoding, which is distinct from one multiplier-adder implemented in MP3 decoding, as claimed in the claim 8. In addition, from section 4.2, 2nd paragraph in Tsai 1, there discloses a MAC for an operation of a synthesis filter bank, which is different from the multiplier-adder for calculating IMDCT and overlap-add, as claimed in the claim 8. As to Tsai 2 and ISO/IEC-3 references, they also fails to disclose one multiplier-adder implemented in MP3 decoding, as claimed in the claim 8. Consequently, according the requirement for establishing a prima facie case of obviousness, Tsai 1, Sakamoto and ISO/IEC-3 fails to disclose all limitations of the independent claims 1 and 8. In brief, according the preceding discussion, , the independent claims 1 and 8 are patentable over "Tsai1" in view of Sakamoto and further in view of ISO/IEC-3. As to the examiner alleged that incorporating the register stack for storing the result produced by IMDCT and a buffer memory for storing the DWIMDCT result into Tsai 1, is obvious to one of ordinary skill in the art and thus concluded that the present invention is "obvious," the proceeding examiner's allegation is made based on the disclosure of the present invention, not on Tsai 1, Sakamoto and ISO/IEC-3 or combinations thereof. Therefore, the examiner's conclusion that the present invention is "obvious," is based on an improper "impermissible hindsight." In other words, the independent claims 1 and 8 are patentable under 35 U.S.C. 103(a).

As per claims 6 and 14

ISO/IEC-3 describes the process of overlapping (dynamic windowing), saying that the second half of the actual block is stored to be used in the next block. This second half is composed of 18 words (for i=0 to 17).

In response thereto, applicants respectfully transverse the aforementioned objections based on the following arguments and thus withdrawal of objections to the claims 6 and 14 is respectfully requested. As described in the proceeding discussion, ISO/IEC-3 fails to disclose where the second half of the actual block to be stored. It would be inappropriate that the examiner presumed that the second half of the actual block to be stored into the same register stack as the present invention because the examiner's presumption has no ground. Even if the examiner's presumption is valid, the register stack of the present invention does function to store the result of IMDCT, rather than the result of the overlap-add operation as disclosed in ISO/IEC-3. Therefore, none of ordinary skill in the art has a motive or desirability to do such combination alleged by the examiner without gleaning the disclosure of the present invention. That is, in view of Tsai1, Sakamoto and further in view of ISO/IEC-3, these references fail to render the claims 6 and 14 obvious. Hence, the claims 6 and 14 are patentable under 35 U.S.C. 103(a).

As per claims 7 and 15

Finally, Tsai 1 and Sakamoto do not teach the modules of INDCT or synthesis filter bank module. However, the ISO/IEC-3 protocal describes these steps to implement the MPEG decoding (IMDCT systhesis and polyphase synthesis, Fig.4)

In response thereto, applicants respectfully transverse the aforementioned objections based on the following arguments and thus withdrawal of objections to the claims 7 and 15 is respectfully requested. First of all, ISO/IEC-3 can't be incorporated into Tsai 1 and Sakamoto as alleged by the examiner because synthesis filterbank disclosed in ISO/IEC-3 is applicable only to the result of IMDCT, instead of being applicable to the results of IMDCT and windowing as disclosed in Sakamoto. As a result, none of ordinary skill in the art has a motive or desirability to incorporating filterbank taught by ISO/IEC-3 into Sakamoto without gleaning the present invention.

That is, the examiner's allegation that ISO/IEC-3 can be incorporated into Tsai 1 and Sakamoto is based on an improper "impermissible hindsight."

In addition, the claims 7 and 15 describe a post process implemented in the hardware structure, wherein the register stack for storing the result produced by IMDCT and the buffer memory for storing the DWIMDCT result are used to realize the post process. However, the

register stack for storing the result produced by IMDCT and the buffer memory for storing the DWIMDCT result are not disclosed in Tsai 1, Sakamoto and ISO/IEC-3 or combinations thereof. Consequently, the claims 7 and 15 are patentable as a matter of law for at least the reason they contain all limitations of their corresponding base independent claims 1 and 8, respectively.

As per the claim 16

Tsai teaches ASIC design (ASIC P 298, PARA 4, line2).

In response thereto, applicants respectfully transverse the aforementioned objections based on the following arguments and thus withdrawal of objections to the claim 16 is respectfully requested. As discussed in the proceeding section, no matter the dependent claim 16 is conventional, the claim 16 is patentable as a matter of law for at least the reason it contains all limitations of its corresponding base independent claim 8.

2. *Claims 2-5 and 10-13 are rejected under 35 U.S.C.103(a) as being unpatentable over "Tsai1" in view of Sakamoto and ISO/IEC-3 as applied to claims 1, 8 and 9 above, and further in view of Tsai (" A novel MPEG-2 audio decoder with efficient data arrangement and memory configuration" hereinafter referred to Tsai 2)*

As per the claims 2 and 10

Tsai 2 teaches the modularized memory for a synthesis window buffer. More Tsai 1 teaches storing data generated by the DWIMDCT module, providing a reading operation of a synthesis subband functions in the post -process stage and writing to and from an IMDCT buffer memory.

In response thereto, applicants respectfully transverse the aforementioned objections based on the following arguments and thus withdrawal of objections to the claims 2 and 10 is respectfully requested. In fact, "Tsai1", Sakamoto and ISO/IEC-3 fail to disclose the register for storing the result of IMDCT and the DWIMDCT buffer memory for storing DWIMDCT result. By contrast, in VI section, 2nd paragraph, 1st sentence in Tsai 2, the systhesis window buffer is used to store the result of a synthesis subband process, which is distinct from the DWIMDCT buffer memory for storing DWIMDCT result in the present invention. Therefore, the systhesis window buffer in Tsai 2 has a distinct function from that of present invention. As a result, the claims 2 and 10 are patentable over "Tsai1" in view of Sakamoto and ISO/IEC-3, as well as Tsai

2.

As per the claims 3 and 11

As per the claims 4 and 12 and

As per the claims 5 and 13:

In response thereto, applicants respectfully transverse the aforementioned objections based on the following arguments and thus withdrawal of objections to the claims 3-5 and 11-13 is respectfully requested.

As discussed in the proceeding section, the dependent claims 3-5 and 11-13 are realized through the provision of the DWIMDCT module and the DWIMDCT buffer memory, as claimed in the independent claims 1 and 8. Therefore, the claims 3-5 and 11-13 are not obvious over "Tsai1" in view of Sakamoto and ISO/IEC-3, (and further in view of Tsai 2) because these references fail to disclose the register for storing the result of IMDCT and the DWIMDCT buffer memory for storing DWIMDCT result. In other words, there is no corresponding register stack or DWIMDCT buffer memory in either of Tsai1, Sakamoto, ISO/IEC-3 and Tsai 2 to perform the same function as the present invention. For example, the claims 3 and 11 disclosed a pipeline structure implementing the register for storing the result of IMDCT and the DWIMDCT buffer memory for storing DWIMDCT result, which is different from that used in Tsai 1. In addition,

the claims 4 and 12 discloses a DWIMDCT buffer memory for storing DWIMDCT result, rather than the synthesis window buffer for storing the result of synthesis subband process in Tsai 2.

Therefore, the claims 3-5 and 11-13 are patentable under 35 U.S.C.103 (a). Furthermore, no matter the dependent claims 3-5 and 11-13 are conventional, they are patentable as a matter of law for at least the reason they contain all limitations of their corresponding base independent claims 1 and 8.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-16 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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Date: 5/3/2005

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